10/020207

COPY

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ATTORNEYS AT LAW

October 19, 2005

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Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Art Unit 2822

Attn: Certification of Corrections Branch

Re: U.S. Utility Patent
Patent No. 6,879,039 B2; Issued: April 12, 2005
For: **Ball Grid Array Package Substrates with a Modified Central Opening and Method for Making the Same**
Inventors: Khan *et al.*
Our Ref: 1875.1640000

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Request for Certification of Correction Under 37 C.F.R. § 1.322;
2. Form PTO/SB/44 (15 pages);
3. Copy of the original Amendment and Reply Under 37 C.F.R. § 1.111 as filed on April 16, 2003, along with a copy of the postcard date-stamped by the USPTO;
4. Copy of the original Form PTO-1449 (20 pages) listing of the cited documents as filed on August 29, 2002, along with a copy of the postcard date-stamped by the USPTO; and
5. One (1) Return Postcard;

It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier. In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Jeffrey S. Weaver
Attorney for Patentees
Registration No. 45,608

JSW/BSW/srb
Enclosures

455446_1.DOC

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent of:	Confirmation No.: 7969
Khan *et al.*	Art Unit: 2822
Patent. No.: 6,879,039 B2	Examiner: Soward, Ida M.
Issued: April 12, 2005	Atty. Docket: 1875.1640000
For: **Ball Grid Array Package Substrates with a Modified Central Opening and Method for Making the Same**	

Request for Certificate of Correction Under 37 C.F.R. § 1.322

Attn: Certificate of Correction Branch

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

It is hereby requested that a Certificate of Correction under 37 C.F.R. § 1.322 be issued for the above-captioned United States Patent. This Certificate of Correction is being requested due to mistakes which appear in the printed patent. These mistakes were made by the U.S. Patent and Trademark Office.

Specifically, the printed patent contains the following errors for which a Certificate of Correction is respectfully requested:

On page 1, the title, "Ball Grid Array Package Substrates and Method of Making the Same," should read as --Ball Grid Array Package Substrates with a Modified Central Opening and Method for Making the Same--.

A copy of the original Amendment and Reply Under 37 C.F.R. § 1.111 as filed on April 16, 2003, along with a copy of the postcard date-stamped by the U.S. Patent and Trademark Office, is enclosed in support of the above correction.

On page 1, the "References Cited" section does not include IDS references submitted on August 29, 2002; and

On page 2 under OTHER PUBLICATIONS, "Kamezos, M., 'An EPBGA Alternative,'" should read as --Karnezos, M., "An EPBGA Alternative,"--.

A copy of the original Form PTO-1449 (20 pages) listing of the cited documents as filed on August 29, 2002, along with a copy of the postcard date-stamped by the U.S. Patent and Trademark Office, is enclosed in support of this correction.

Remarks

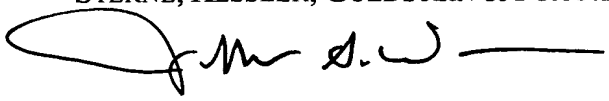
The above-noted corrections do not involve such changes in the patent as would constitute new matter or would require reexamination.

A completed Form PTO/SB/44 accompanies this request, with the above-noted corrections printed thereon. Accordingly, a Certificate of Correction is believed proper and issuance thereof is respectfully requested.

The Commissioner is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.



Jeffrey S. Weaver
Attorney for Patentees
Registration No. 45,608

Date: October 19, 2005

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,879,039 B2

APPLICATION NO.: 10/020,207

ISSUE DATE : April 12, 2005

INVENTOR(S) : Reza-Ur Rahman Khan

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On page 1, the title, "Ball Grid Array Package Substrates and Method of Making the Same," should read as --Ball Grid Array Package Substrates with a Modified Central Opening and Method for Making the Same--.

On page 1, in the "References Cited" section, please insert the following references under "U.S. PATENT DOCUMENTS" as cited on the PTO-1449 Form submitted on August 29, 2002:

5,397,921	03/1995	Karnezos
5,474,957	12/1995	Urushima
5,534,467	07/1996	Rostoker
09/984,259	---	Zhao et al.
09/997,272	---	Zhao et al.
09/742,366	---	Khan et al.

On page 1, in the "References Cited" section, please insert the following references under "FOREIGN PATENT DOCUMENTS" as cited on the PTO-1449 Form submitted on August 29, 2002:

EP 0 504 411 B1 06/1998

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On page 1, in the "References Cited" section, please insert the following references under "OTHER PUBLICATIONS" as cited on the PTO-1449 Form submitted on August 29, 2002:

Ahn, S.H. and Kwon, Y.S., "Popcorn Phenomena in a Ball Grid Array Package", IEEE Transactions on Components, Packaging, and Manufacturing Technology Part B: Advanced Packaging, IEEE, August 1995, Vol. 18, No. 3, pp. 491-96.

Amkor Electronics, "Amkor BGA Packaging: Taking The World By Storm", Electronic Packaging & Production, Cahners Publishing Company, May 1994, page unknown.

Anderson, L. and Trabucco, B., "Solder Attachment Analysis of Plastic BGA Modules", Surface Mount International Conference, Surface Mount International, August 28-September 1, 1994, San Jose, California, pp. 189-194.

Andrews, M., "Trends in Ball Grid Array Technology," Ball Grid Array National Symposium, March 29-30, 1995, Dallas, Texas, 10 pages.

Attarwala, A.I. Dr. and Stierman, R., "Failure Mode Analysis of a 540 Pin Plastic Ball Grid Array", Surface Mount International Conference, Surface Mount International, August 28-September 1, 1994, San Jose, California, pp. 252-257.

Banerji, K., "Development of the Slightly Larger Than IC Carrier (SLICC), Journal of Surface Mount Technology, July 1994, pp. 21-26.

Bauer, C., Ph.D., "Partitioning and Die Selection Strategies for Cost Effective MCM Designs", Journal of Surface Mount Technology, October 1994, pp. 4-9.

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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Bernier, W.E. et al., "BGA vs. QFP: A Summary of Tradeoffs for Selection of High I/O Components", Surface Mount International Conference Proceedings, Surface Mount International, August 28-September 1, 1994, San Jose, California, pp. 181-185.

Burgos, J. et al., "Achieving Accurate Thermal Characterization Using a CFD Code -- A Case Study of Plastic Packages", IEEE Transactions on Components, Packaging, and Manufacturing Technology Part A, IEEE, December 1995, Vol. 18, No. 4, pp. 732-738.

Chadima, M., "Interconnecting Structure Manufacturing Technology," Ball Grid Array National Symposium, Dallas, Texas, March 29-30, 1995.

Chanchani, R. et al., "Mini BGA: Pad and Pitch Ease Die Test and Handling", Advanced Packaging, IHS Publishing Group, May/June 1995, pp.34, 36-37.

Chung, T.C. et al., "Rework of Plastic, Ceramic, and Tape Ball Grid Array Assemblies", Ball Grid Array National Symposium Proceedings, Dallas, Texas, March 29-30, 1995, pp. 1-15.

Cole, M.S. and Caulfield, T. "A Review of Available Ball Grid Array (BGA) Packages", Journal of Surface Mount Technology, Surface Mount Technology Association, January 1996, Vol. 9, pp. 4-11.

Cole, M.S. and Caulfield, T., "Ball Grid Array Packaging", Surface Mount International Conference Proceedings, Surface Mount International, August 28-September 1, 1994, San Jose, California, pp. 147-153.

Dobers, M. and Seyffert, M., "Low Cost MCMs: BGAs Provide a Fine-Pitch Alternative", Advanced Packaging, IHS Publishing Group, September/October 1994, Vol. 3, No. 5, pp. 28, 30 and 32.

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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Dody, G. and Burnette, T., "BGA Assembly Process and Rework", Journal of Surface Mount Technology, Surface Mount Technology Association, January 1996, Vol. 9, pp. 39-45.

Edwards, D. et al., "The Effect of Internal Package Delaminations on the Thermal Performance of PQFP, Thermally Enhanced PQFP, LOC and BGA Packages", 45th Electronic Components & Technology Conference, IEEE, May 21-24, 1995, Las Vegas, NV, pp. 285-292.

Ejim, T.L. et al., "Designed Experiment to Determine Attachment Reliability Drivers for PBGA Packages", Journal of Surface Mount Technology, Surface Mount Technology Association, January 1996, Vol. 9, pp. 30-38.

Ewanich, J. et al., "Development of a Tab (TCP) Ball Grid Array Package", Proceedings of the 1995 International Electronics Packaging Conference, San Diego, CA, September 24-27, 1995, pp. 588-594.

Fauser, S. et al, "High Pin-Count PBGA Assembly", Circuits Assembly, February 1995, Vol 6, No. 2, pp. 36-38 and 40.

Fauser, Suzanne et al., "High Pin-Count PBGA Assembly: Solder Defect Failure Modes and Root Cause Analysis", Surface Mount International, Proceedings of The Technical Program, Surface Mount International, August 28-September 1, 1994, San Jose, California, pp. 169-174.

Ferguson, M. "Ensuring High-Yield BGA Assembly", Circuits Assembly, February 1995, Vol. 6, No. 2, pp. 54, 56 and 58.

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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Freda, M., "Laminate Technology for IC Packaging", Electronic Packaging & Production, Cahners Publishing Company, October 1995, Vol. 35, No. 11, pp. S4-S5.

Freedman, M., "Package Size and Pin-Out Standardization", Ball Grid Array National Symposium, March 29-30, 1995, 7 pages.

Freyman, B. and Pennisi, R., "Over-molded Plastic Pad Arrary Carriers (OMPAC): A Low Cost, High Interconnect Density IC Packaging Solution for Consumer and Industrial Electronics", 41st Electronic Components & Technology Conference, IEEE, May 11-16, 1991, pp. 176-82.

Freyman, B. et al., "Surface Mount Process Technology for Ball Grid Array Packaging", Surface Mount International Conference Proceedings, Surface Mount International, August 29-September 2, 1993, San Jose, California, pp. 81-85.

Freyman, B. et al., "The Move to Perimeter Plastic BGAs", Surface Mount International Conference Proceedings, San Jose, CA, August 29-31, 1995, pp. 373-382.

Freyman, B., "Trends in Plastic BGA Packaging," Ball Grid Array National Symposium, Dallas, Texas, March 29-30, 1995, 45 pages.

Gilleo, K., "Electronic Polymers: Die Attach and Oriented Z-Axis Films", Advanced Packaging, IHS Publishing Group, September/October 1994, Vol. 3, No. 5, pp. 37-38, 40 and 42.

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Guenin, B. et al., "Analysis of a Thermally Enhanced Ball Grid Array Package", IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part A, IEEE Components, Packaging, and Manufacturing Technology Society, December 1995, Vol. 18, No. 4, pp. 749-757.

Hart, C., "Vias in Pads for Coarse and Fine Pitch Ball Grid Arrays", Surface Mount International Conference Proceedings, Surface Mount International, August 28-September 1, 1994, San Jose, California, pp. 203-207.

Hart, C. "Vias in Pads", Circuits Assembly, February 1995, Vol. 6, No. 2, pp. 42, 44-46 and 50.

Hattas, D., "BGAs Face Production Testing: New Package Offers Promise but Must Clear Technology Hurdles.", Advanced Packaging, IHS Publishing Group, Summer 1993, Vol. 2, No. 3, pp. 44-46.

Heitmann, R., "A Direct Attach Evolution: TAB, COB and Flip Chip Assembly Challenges", Advanced Packaging, IHS Publishing Group, July/August 1994, Vol. 3, No. 4, pp. 95-99 and 103.

Hodson, T., "Study Examines BGA Use", Electronic Packaging & Production, March 1993, page unknown.

Holden, H., "The Many Techniques of Small Via Formation for Thin Boards", The Institute for Interconnecting and Packaging Electronic Circuits Ball Grid Array National Symposium, San Diego, CA, January 18-19, 1996, pp. 1-7.

Houghten, J., "New Package Takes On QFPs", Advanced Packaging, IHS Publishing Group, Winter 1993, Vol. 2, No. 1, pp. 38-39.

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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

"How To Give Your BGAs A Better Bottom Line.", Advanced Packaging, IHS Publishing Group, January/February 1995, page unknown.

Huang, W. and Ricks, J.,"Electrical Characterization of PBGA for Communication Applications by Simulation and Measurement", National Electronic Packaging and Production Conference West '95, February 26-March 2, 1995, Anaheim, California, pp. 300-307.

Hundt, M. et al., "Thermal Enhancements of Ball Grid Arrays", National Electronic Packaging and Production Conference West '95, Reed Exhibition Companies, Anaheim, CA, February 25-29, 1996, pp. 702-711.

Hutchins, C.L., "Understanding Grid Array Packages", Surface Mount Technology Magazine, IHS Publishing Group, November 1994, Vol. 8, No. 11, pp. 12-13.

Hwang, J.S., "Reliability of BGA Solder Interconnections", Surface Mount Technology Magazine, IHS Publishing Group, September 1994, Vol. 8, No. 9, pp. 14-15.

Hwang, J.S., "A Hybrid of QFP and BGA Architectures", Surface Mount Technology Magazine, IHS Publishing Group, February 1995, Vol. 9, No. 2, p. 18.

Johnson, R. et al., "A Feasibility Study of of Ball Grid Array Packaging", National Electronic Packaging and Production Conference East '93, Boston, Massachusetts, June 14-17, 1993, pp. 413-422.

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Johnson, R. et al., "Thermal Characterization of 140 and 225 Pin Ball Grid Array Packages", National Electronic Packaging & Production Conference East '93, Boston, Massachusetts, June 14-17, 1993, pp. 423-430.

Johnston, P., "Land Pattern Interconnectivity Schemes", Ball Grid Array National Symposium, Dallas, Texas, March 29-30, 1995, pages 2-21.

Johnston, P. "Printed Circuit Board Design Guidelines for Ball Grid Array Packages", Journal of Surface Mount Technology, Surface Mount Technology Association, January 1996, Vol. 9, pp. 12-18.

Kawahara, T. et al., "Ball Grid Array Type Package By Using of New Encapsulation Method", Proceedings of the 1995 International Electronics Packaging Conference, San Diego, CA, September 24-27, 1995, pp. 577-587.

Knickerbocker, J.U. and Cole, M.S., "Ceramic BGA: A Packaging Alternative", Advanced Packaging, IHS Publishing Group, January/February 1995, Vol. 4, No. 1, pp. 20, 22 and 25.

Kromann, G., et al., "A Hi-Density C4/CBGA Interconnect Technology for a CMOS Microprocessor", National Electronic Packaging and Production Conference West '95, IEEE, February 26-March 2, 1995, Anaheim, California, pp. 1523-1529.

Kunkle, R., "Discrete Wiring for Array Packages", Ball Grid Array National Symposium, Dallas, Texas, March 29-30, 1995, 9 pages.

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Lall, B. et al, "Methodology for Thermal Evaluation of Multichip Modules", IEEE Transactions on Components, Packaging, and Manufacturing Technology Part A, IEEE, December 1995, Vol. 18, No. 4, pp. 758-764.

Lasance, C. et al., "Thermal Characterization of Electronic Devices with Boundary Condition Independent Compact Models", IEEE Transactions on Components, Packaging, and Manufacturing Technology Part A, IEEE Components, Packaging, and Manufacturing Technology Society, December 1995, Vol. 18, No. 4, pp. 723-731.

Lau, J., "Ball Grid Array Technology", McGraw Hill Inc., 1995, entire book submitted.

Lau, J. et al., "No Clean Mass Reflow of Large Plastic Ball Grid Array Packages", Circuit World, Wela Publications Ltd., Vol. 20, No. 3, March 1994, pp.15-22.

"Literature Review", Special Supplement to Electronic Packaging & Production, February 1995, Cahners Publication, 10 pages.

LSI LOGIC Package Selector Guide, Second Edition, LSI Logic Corporation, 1994-1995, entire document submitted.

"LTCC MCMs Lead to Ceramic BGAs," Advanced Packaging, IHS Publishing Group, September/October 1994, Vol. 3, No. 5, pp. 14-15.

Mak, Dr. W.C. et al., "Increased SOIC Power Dissipation Capability Through Board Design and Finite Element Modeling", Journal of Surface Mount Technology, Surface Mount International, October 1994, pp. 33-41.

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Marrs, R.C. and Olachea, G., "BGAs For MCMs: Changing Markets and Product Functionality", Advanced Packaging, IHS Publishing Group, September/October 1994, Vol. 3, No. 5, pp. 48, 50, and 52.

Matthew, L.C. et al., "Area Array Packaging: KGD in a Chip-Sized Package", Advanced Packaging, IHS Publishing Group, July/August 1994, pp. 91-94.

Mawer, A. et al., "Plastic BGA Solder Joint Reliability Considerations", Surface Mount International Conference Proceedings, Surface Mount International, August 28-September 1, 1994, San Jose, California, pp. 239-251.

Mazzullo, T. and Schaertl, L., "How IC Packages Affect PCB Design", Surface Mount Technology Magazine, February 1995, Vol. 9, No. 2, pp. 114-116.

Mearig, J., "An Overview of Manufacturing BGA Technology", National Electronic Packaging and Production Conference West '95, February 26-March 2, 1995, Anaheim, California, pp. 295-299.

Mertol, A., "Application of the Taguchi Method on the Robust Design of Molded 225 Plastic Ball Grid Array Packages", IEEE Transactions on Components, Packaging, and Manufacturing Technology Part B: Advanced Packaging, IEEE, November 1995, Vol. 18, No. 4, pp. 734-743.

Mescher, P. and Phelan, G., "A Practical Comparison of Surface Mount Assembly for Ball Grid Array Components", Surface Mount International Conference Proceedings, Surface Mount International, August 28-September 1, 1994, San Jose, California, pp. 164-168.

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Mulgaonker, S. et al., "An Assessment of the Thermal Performance of the PBGA Family", Eleventh Annual IEEE Semiconductor Thermal Measurement and Management Symposium, IEEE, San Jose, CA, February 7-9, 1995, pp. 17-27.

"New PBGA Pushes Technology to Outer Limits", Advanced Packaging, IHS Publishing Group, January/February 1995, page 11.

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Ramirez, C. and Fauser, S., "Fatigue Life Comparison of The Perimeter and Full Plastic Ball Grid Array", Surface Mount International Conference Proceedings, Surface Mount International, August 28-September 1, 1994, San Jose, California, pp. 258-266.

Rogren, P., "MCM-L Built on Ball Grid Array Formats", National Electronic Packaging and Production Conference West '94, Anaheim, California, pp. 1277-1282.

MAILING ADDRESS OF SENDER (Please do not use customer number below):

Sterne, Kessler, Goldstein & Fox P.L.L.C.
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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,879,039 B2

APPLICATION NO.: 10/020,207

ISSUE DATE : April 12, 2005

INVENTOR(S) : Reza-Ur Rahman Khan

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Rooks, S., "X-Ray Inspection of Flip Chip Attach Using Digital Tomosynthesis", Surface Mount International, Proceedings of The Technical Program, August 28-September 1, 1994, San Jose, California, pp. 195-202.

Rukavina, J., "Attachment Methodologies: Ball Grid Array Technology", Ball Grid Array National Symposium, Dallas, Texas, March 29-30, 1995, 37 pages.

Sack, T., "Inspection Technology", Ball Grid Array National Symposium, Dallas, Texas, March 29-30, 1995, pages 1-41.

Sakaguchi, H., "BGA Mounting Technology," pgs. 1-4, date and source unknown.

Schmolze, C. and Fraser, A., "SPICE Modeling Helps Enhance BGA Performance", Electronic Packaging & Production, January 1995, pp. 50-52.

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Shimizu, J., "Plastic Ball Grid Array Coplanrity", Surface Mount International Conference, San Jose, California, August 31-September 2, 1993, pp. 86-91.

Sigliano, R., "Using BGA Packages: An Appealing Technology in a QFP and Fine-Pitch Market", Advanced Packaging, IHS Publishing Group, March/April 1994, pp. 36-39.

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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Sirois, L., "Dispensing for BGA: Automated Liquid Dispensing in a High-Density Environment", Advanced Packaging, IHS Publishing Group, May/June 1995, pp. 38 and 41.

Solberg, V., "Interconnection Structure Preparation: Impact of Material Handling and PCB Surface Finish on SMT Assembly Process Yield", Ball Grid Array National Symposium, Dallas, Texas, March 29-30, 1995, 10 pages.

"Survival of the Fittest", Advanced Packaging, IHS Publishing Group, March/April 1995, page unknown.

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Walshak, D. and Hashemi, H., "Thermal Modeling of a Multichip BGA Package", National Electronic Packaging and Production Conference West '94, Reed Exhibition Companies, Anaheim, California, February 27-March 4, 1994, pp. 1266-1276.

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PATENT NO. : 6,879,039 B2

APPLICATION NO.: 10/020,207

ISSUE DATE : April 12, 2005

INVENTOR(S) : Reza-Ur Rahman Khan

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Walshak, D. and Hashemi, H., "BGA Technology: Current and Future Direction for Plastic, Ceramic and Tape BGAs", Surface Mount International Conference Proceedings, Surface Mount International, August 28-September 1, 1994, San Jose, California, pp. 157-163.

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Zamborsky, E., "BGAs in the Assembly Process", Circuits Assembly, February 1995, Vol. 6, No. 2, pp. 60, 62-64.

Zimerman, M., "High Performance BGA Molded Packages for MCM Application", Surface Mount International Conference Proceedings, Surface Mount International, August 28-September 1, 1994, San Jose, California, pp. 175-180.

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PATENT NO. : 6,879,039 B2

APPLICATION NO.: 10/020,207

ISSUE DATE : April 12, 2005

INVENTOR(S) : Reza-Ur Rahman Khan

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Zweig, G., "BGAs: Inspect the Process, Not the Product", Electronic Packaging & Production (Special Supplement), Cahners Publishing Company, August 1994 (Supplement), p. 41.

Houghten, J.L., "Plastic Ball-Grid Arrays Continue To Evolve", Electronic Design, February 6, 1995, pp. 141-146.

Marrs, R. et al., "Recent Technology Breakthroughs Achieved with the New *Super*BGA® Package", 1995 International Electronics Packaging Conference, San Diego, California, September 24-27, 1995, pp. 565-576.

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Thompson, T., "Reliability Assessment of a Thin (Flex) BGA Using a Polyimide Tape Substrate", Internationsl Electronics Manufacturing Technology Symposium, IEEE, 1999, pp. 207-213.

On page 2 under OTHER PUBLICATIONS, "Kamezos, M., 'An EPBGA Alternative,'" should read as --Karnezos, M., "An EPBGA Alternative,"--.

MAILING ADDRESS OF SENDER (Please do not use customer number below):

Sterne, Kessler, Goldstein & Fox P.L.L.C.
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Washington, DC 20005-3934

		Due Date:	April 16, 2003
Applicant:	Khan *et al.*	**Art Unit:**	2822
		Examiner:	Soward, Ida M.
Application No.:	10/020,207	**Docket:**	1875.1640000
Filed:	December 18, 2001	**Atty:**	RES/JSW

For: **Ball Grid Array Package Substrates with a Modified Central Opening and Method for Making the Same** (as amended)

When receipt stamp is placed hereon, the USPTO acknowledges receipt of the following documents:

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.: 7969
Khan *et al.*	Art Unit: 2822
Appl. No. 10/020,207	Examiner: Soward, Ida M.
Filed: December18, 2001	Atty. Docket: 1875.1640000
For: **Ball Grid Array Package Substrates with a Modified Central Opening and Method for Making the Same (as amended)**	

Amendment And Reply Under 37 C.F.R. § 1.111

Commissioner for Patents
Washington, D.C. 20231

Sir:

In reply to the Office Action dated **January 16, 2003**, (PTO Prosecution File Wrapper Paper No. 7), Applicants submit the following Amendment and Remarks. This Amendment is provided in the following format:

(A) A clean version of each replacement paragraph/section/claim along with clear instructions for entry;

(B) Starting on a separate page, appropriate remarks and arguments. 37 C.F.R. § 1.121 and MPEP 714; and

(C) Starting on a separate page, a marked-up version entitled: "Version with markings to show changes made."

It is not believed that extensions of time or fees for net addition of claims are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent

abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to our Deposit Account No. 19-0036.

Amendments

In the Title:

Kindly change the title from "Ball Grid Array Package Substrates and Method for Making the Same" to --Ball Grid Array Package Substrates with a Modified Central Opening and Method for Making the Same--.

In the Claims:

Please substitute the following claim 1, 2, 8-10, 13-15, 18, 19, 22, and 25 for the pending claim 1, 2, 8-10, 13-15, 18, 19, 22, and 25:

1. (Amended) A substrate in an integrated circuit (IC) package, comprising:

opposing first and second surfaces, wherein one of said first and said second surfaces has a plurality of solder ball contacts pads formed thereon, wherein said first surface has a central opening,

wherein said central opening has an edge,

wherein said edge includes at least one protruding edge portion that extends into said central opening,

whereby said at least one protruding edge portion provides a shorter distance between a trace on said first surface and an IC die relative to a distance between the trace and the IC die when said at least one protruding edge portion is not present.

2. (Amended) The substrate of claim 1, wherein the substrate is capable of being coupled to a surface of a stiffener that has a central bondable ring, wherein said at least one protruding edge portion is configured to extend across a portion of the central bondable ring when the substrate is coupled to the stiffener surface.

8. (Amended) A substrate in an integrated circuit (IC) package, comprising:

opposing first and second surfaces, wherein one of said first and said second surfaces has a plurality of solder ball contacts pads formed thereon, wherein said first surface has a central opening,

wherein said central opening has an edge,

wherein said edge includes at least one recessed edge portion,

whereby said at least one recessed edge portion provides access to a portion of a surface of a stiffener attached to the substrate relative to when the at least one recessed edge portion is not present.

9. (Amended) The substrate of claim 8, wherein the substrate is capable of being coupled to a surface of a stiffener that has a central bondable ring, wherein said at least one recessed edge portion is configured to expose a portion of the central bondable ring when the substrate is coupled to the stiffener surface.

10. (Amended) The substrate of claim 9, wherein said at least one recessed edge portion is configured to allow a corresponding bond wire to couple an IC die mounted on said surface of said stiffener to said central bondable ring.

13. (Amended) A substrate in an integrated circuit (IC) package, comprising:

opposing first and second surfaces, wherein one of said first and said second surfaces has a plurality of solder ball contacts pads formed thereon, wherein said first surface has a central opening,

wherein said central opening has an edge,

wherein said first surface includes at least one hole proximate to said edge,

whereby said at least one hole proximate to said edge provides access to a portion of a surface of a stiffener attached to the substrate relative to when the at least one hole proximate to said edge is not present.

14. (Amended) The substrate of claim 13, wherein the substrate is capable of being coupled to a surface of a stiffener that has a central bondable ring, wherein said

at least one hole is configured to expose a portion of the central bondable ring when the substrate is coupled to the stiffener surface.

15. (Amended) The substrate of claim 14, wherein said at least one hole is configured to allow a corresponding bond wire to couple an IC die mounted on said surface of said stiffener to the exposed portion of the central bondable ring.

18. (Amended) A substrate in an integrated circuit (IC) package, comprising:

opposing first and second surfaces, wherein one of said first and said second surfaces has a plurality of solder ball contacts pads formed thereon, wherein said first surface of the substrate has a central opening, wherein said central opening has an edge;

a first trace on said first surface of the substrate proximate to a first portion of said edge;

a second trace on said first surface of the substrate proximate to a second portion of said edge;

wherein the substrate is capable of being coupled to a surface of a stiffener that has a central bondable ring, wherein said first portion of said edge is configured to cover a first portion of the central bondable ring when the substrate is coupled to the surface of the stiffener, and said second portion of said edge is configured to expose a second portion of the central bondable ring when the substrate is coupled to the surface of the stiffener;

whereby said first portion of said edge allows for a shorter distance between said first trace and an IC die relative a distance between said second trace and the IC die.

19. (Amended) The substrate of claim 18, wherein said second portion of said edge is configured to allow a wire to couple an IC die to the second portion of the central bondable ring.

22. (Amended) An integrated circuit (IC) package, comprising:

a substrate that has opposing first and second surfaces, wherein one of said first and said second surfaces has a plurality of solder ball contact pads formed thereon, wherein said first surface has a central opening;

a stiffener that has a first surface, wherein said first surface of said stiffener has a central bondable ring, wherein said first surface of said stiffener is attached to said substrate;

wherein said central opening has an edge, wherein said edge includes at least one of:

(a) a protruding edge portion that extends across at least a portion of said central ground ring,

(b) a recessed edge portion that exposes a portion of said central ground ring, or

(c) a hole proximate to said edge, wherein the hole exposes a portion of said central ground ring.

25. (Amended) The IC package of claim 22, wherein said first surface of said stiffener has a central cavity that coincides with said central opening of said substrate, wherein said central bondable ring surrounds said central cavity.

Please add the following claims:

31. (New) The substrate of claim 2, wherein the central bondable ring is a ground ring or a power ring.

32. (New) The substrate of claim 9, wherein the central bondable ring is a ground ring or a power ring.

33. (New) The substrate of claim 14, wherein the central bondable ring is a ground ring or a power ring.

34. (New) The substrate of claim 18, wherein the central bondable ring is a ground ring or a power ring.

35. (New) The IC package of claim 22, wherein said central bondable ring is a ground ring or a power ring.

36. (New) An integrated circuit (IC) package, comprising:

a stiffener that has a first surface, wherein said first surface of said stiffener has a central bondable ring;

an IC die mounted to said first surface of said stiffener within said central bondable ring; and

a substrate that has opposing first and second surfaces, wherein said first surface of said substrate has a plurality of solder ball contact pads formed thereon, wherein said first surface of said stiffener is attached to said second surface of said substrate, wherein said substrate has a central opening that is open at said first and said second surfaces of said substrate, wherein the central opening accommodates said IC die;

wherein said central opening has an edge, wherein said edge has a protruding edge portion that extends across a portion of said central bondable ring, wherein a trace on said first surface of said substrate extends into said protruding edge portion;

whereby said protruding edge portion provides a shorter distance between said trace and said IC die relative a distance between said trace and said IC die when said protruding edge portion is not present.

37. (New) The IC package of claim 36, further comprising:

a bond wire that couples a pin of said IC die to said trace.

38. (New) The IC package of claim 36, further comprising:

a bond wire that couples a pin of said IC die to said central bondable ring.

39. (New) An integrated circuit (IC) package, comprising:

a stiffener that has a first surface, wherein said first surface of said stiffener has a central bondable ring;

an IC die mounted to said first surface of said stiffener within said central bondable ring;

a substrate that has opposing first and second surfaces, wherein said first surface of said substrate has a plurality of solder ball contact pads formed thereon, wherein said first surface of said stiffener is attached to said second surface of said substrate, wherein said substrate has a central opening that is open at said first and said second surfaces of said substrate, wherein said central opening accommodates said IC die; and

wherein said central opening has an edge, wherein said edge has a recessed edge portion that exposes a portion of said central bondable ring;

whereby said recessed edge portion provides access to a portion of said central bondable ring that would not be accessible when the recessed edge portion is not present.

40. (New) The IC package of claim 39, further comprising:

a bond wire that couples a pin of said IC die to a trace on said first surface of said substrate proximate to said edge.

41. (New) The IC package of claim 39, further comprising:

a bond wire that couples a pin of said IC die to said portion of central bondable ring exposed by said recessed edge portion.

42. (New) An integrated circuit (IC) package, comprising:

a stiffener that has a first surface, wherein said first surface of said stiffener has a central bondable ring;

an IC die mounted to said first surface of said stiffener within said central bondable ring; and

a substrate that has opposing first and second surfaces, wherein said first surface of said substrate has a plurality of solder ball contact pads formed thereon, wherein said first surface of said stiffener is attached to said second surface of said substrate, wherein said substrate has a central opening that is open at said first surface and said second surface of said substrate, wherein said central opening accommodates said IC die, wherein said first surface of said substrate has a hole proximate to an edge of said central opening;

wherein said hole exposes a portion of said central bondable ring;

whereby said hole provides access to said portion of said central bondable ring that would not be accessible when said hole is not present.

43. (New) The IC package of claim 42, further comprising:

a bond wire that couples a pin of said IC die to a trace on said first surface of said substrate proximate to said edge.

44. (New) The IC package of claim 42, further comprising:

a bond wire that couples a pin of said IC die to said portion of central bondable ring through said hole.

45. (New) The substrate of claim 2, wherein said plurality of solder ball contact pads are on said first surface of the substrate.

46. (New) The substrate of claim 2, wherein said plurality of solder ball contact pads are on said second surface of the substrate.

47. (New) The substrate of claim 9, wherein said plurality of solder ball contact pads are on said first surface of the substrate.

48. (New) The substrate of claim 9, wherein said plurality of solder ball contact pads are on said second surface of the substrate.

49. (New) The substrate of claim 14, wherein said plurality of solder ball contact pads are on said first surface of the substrate.

50. (New) The substrate of claim 14, wherein said plurality of solder ball contact pads are on said second surface of the substrate.

51. (New) The substrate of claim 18, wherein said plurality of solder ball contact pads are on said first surface of the substrate.

52. (New) The substrate of claim 18, wherein said plurality of solder ball contact pads are on said second surface of the substrate.

53. (New) The substrate of claim 22, wherein said plurality of solder ball contact pads are on said first surface of the substrate.

54. (New) The substrate of claim 22, wherein said plurality of solder ball contact pads are on said second surface of the substrate.

Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 1-27 and 31-54 are pending in the application, with 1, 8, 13, 18, 22, 36, 39, and 42 being the independent claims. Claims 1, 2, 8-10, 13-15, 18, 19, 22, and 25 are sought to be amended. The amendments to claims 1, 2, 8-10, 13-15, 18, 19, 22, and 25 are made to more particularly claim the present invention, not to amend around cited art, and are thus not intended to limit the range of any equivalents. New claims 31-54 are sought to be added. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Examiner Interview

Applicants would like to thank Examiner Soward for the courteous Examiner Interview conducted at the U.S. Patent and Trademark Office on April 2, 2003, with Applicants' representative Jeffrey S. Weaver, Reg. No. 45,608.

Objection to the Title

The Examiner has objected to the current title of the application and required Applicants to revise it. Applicants have amended the title to better reflect the claimed

invention. Accordingly, Applicants respectfully request that the Examiner reconsider and withdraw this objection.

Rejections under 35 U.S.C. § 102

Claims 1-8, 13, 16, and 17 have been rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,020,637 to Karnezos (hereinafter Karnezos). Applicants respectfully traverse the rejection, and request that it be withdrawn.

Technical differences exist between Karnezos and the present invention. Independent claims 1, 8, and 13 of the present invention relate to substrates in integrated circuit (IC) packages. Claims 1, 8, and 13, as amended, each recite that the substrate has opposing first and second surfaces, that one of the first and second surfaces has a plurality of solder ball contacts pads formed thereon, wherein the first surface has a central opening, and the central opening has an edge.

Independent claim 1 recites the edge including at least one protruding edge portion that extends into the central opening. Independent claim 8 recites the edge including at least one recessed edge portion. Independent claim 13 recites the first surface of the substrate including at least one hole proximate to the edge of the central opening. Karnezos does not teach or even suggest these features of independent claims 1, 8, and 13.

Accordingly, Applicants respectfully submit that independent claims 1, 8, and 13 are patentable over Karnezos, for at least these reasons. Furthermore, new independent claims 36, 39, and 42 are patentable over Karnezos for at least the same reasons. Claims 2-7, 16, 17, and new claims 31, 37, 38, 40, 41, and 43-46, which depend therefrom, are

also patentable for at least these reasons, and further in view of their own features. Applicants therefore request that the Examiner reconsider and withdraw the rejection of these claims.

Rejections under 35 U.S.C. § 103

Claims 9-12, 14, 15, and 18-27 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Karnezos in view of U.S. Publication No. 2002/0072214 A1 to Yazawa *et al.* (hereinafter Yazawa). Applicants respectfully traverse the rejection, and request that it be withdrawn.

For at least the reasons described above, claims 1-8, 13, 16, and 17 are patentable over Karnezos. Furthermore, Applicants assert that Yazawa does not supply the missing teachings. Thus, claims 9-12, 14, and 15, and new claims 32, 33, and 47-50, which depend from claims 9 and 14, are also patentable over Karnezos and Yazawa, alone or in combination, for at least these reasons, and further in view of their own features.

Furthermore, Applicants assert that independent claim 22 is patentable over Karnezos and Yazawa, alone or in combination, for at least the reasons described above relating to independent claims 1, 8, and 13, and further in view of its own features. Claims 23-27, and new claims 35, 53, and 54, which depend from claim 22, are also patentable over Karnezos and Yazawa, alone or in combination, for at least these reasons, and further in view of their own features.

Technical differences exist between claim 18 of the present invention, and Karnezos and/or Yazawa. Independent claim 18 relates to a substrate in an integrated circuit (IC) package. As recited in claim 18, one of opposing first and second surfaces of

the substrate has a plurality of solder ball contacts pads formed thereon. As further recited in claim 18, the first surface of the substrate has a central opening, and the central opening has an edge. As further recited in claim 18, a first portion of the edge is configured to cover a first portion of a central bondable ring of a stiffener when the substrate is coupled to the surface of the stiffener, and a second portion of the edge is configured to expose a second portion of the central bondable ring when the substrate is coupled to the surface of the stiffener. Karnezos, alone or in combination with Yazawa, does not teach or even suggest this feature of independent claim 18.

Accordingly, Applicants respectfully submit that independent claim 18 is patentable over Karnezos and Yazawa, alone or in combination, for at least these reasons. Claims 19-21, and new claims 34, 51, and 52, which depend from claim 18, are also patentable for at least these reasons, and further in view of their own features.

Applicants therefore request that the Examiner reconsider and withdraw the rejection of claims 9-12, 14, 15, and 18-27.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will

expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Jeffrey S. Weaver
Attorney for Applicants
Registration No. 45,608

Date: 4-16-03

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Applicant: Khan et al.

Application No.: 10/020,207

Filed: December 18, 2001

For: **Ball Grid Array Package Substrates and Method of Making the Same**

Due Date: N/A

Art Unit: 2811

Examiner: To Be Assigned

Docket: 1875.1640000

Atty: JSW

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INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO. 1875.1640000	APPLICATION NO. 10/020,207
APPLICANT Khan *et al.*	
FILING DATE December 18, 2001	GROUP 2811

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA1	5,397,921	03/1995	Karnezos	257	779	
	AB1	5,474,957	12/1995	Urushima	437	209	
	AC1	5,534,467	07/1996	Rostoker	437	209	
	AD1	09/984,259	---	Zhao et al.	---	---	10/29/2001
	AE1	09/997,272	---	Zhao et al.	---	---	11/30/2001
	AF1	09/742,366	---	Khan et al.	---	---	12/22/2000
	AG1						
	AH1						
	AI1						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ1	EP 0 504 411 B1	06/1998	EPO	H01L	23/04	Yes No
	AK1						Yes No
	AL1						Yes No
	AM1						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	1	Ahn, S.H. and Kwon, Y.S., "Popcorn Phenomena in a Ball Grid Array Package", IEEE Transactions on Components, Packaging, and Manufacturing Technology Part B: Advanced Packaging, IEEE, August 1995, Vol. 18, No. 3, pp. 491-96.
	AO	1	Amkor Electronics, "Amkor BGA Packaging: Taking The World By Storm", Electronic Packaging & Production, Cahners Publishing Company, May 1994, page unknown.
	AP	1	Anderson, L. and Trabucco, B., "Solder Attachment Analysis of Plastic BGA Modules", Surface Mount International Conference, Surface Mount International, August 28-September 1, 1994, San Jose, California, pp. 189-194.
	AQ	1	Andrews, M., "Trends in Ball Grid Array Technology," Ball Grid Array National Symposium, March 29-30, 1995, Dallas, Texas, 10 pages.
	AR	1	Attarwala, A.I. Dr. and Stierman, R., "Failure Mode Analysis of a 540 Pin Plastic Ball Grid Array", Surface Mount International Conference, Surface Mount International, August 28-September 1, 1994, San Jose, California, pp. 252-257.

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FORM PTO-1449 ~~INFORMATION DISCLOSURE STATEMENT~~	ATTY. DOCKET NO. 1875.1640000	APPLICATION NO. 10/020,207
	APPLICANT Khan *et al.*	
	FILING DATE December 18, 2001	GROUP 2811

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA2						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ2						Yes No
	AK2						Yes No
	AL2						Yes No
	AM2						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	2	Banerji, K., "Development of the Slightly Larger Than IC Carrier (SLICC), Journal of Surface Mount Technology, July 1994, pp. 21-26.
	AO	2	Bauer, C., Ph.D., "Partitioning and Die Selection Strategies for Cost Effective MCM Designs", Journal of Surface Mount Technology, October 1994, pp. 4-9.
	AP	2	Bernier, W.E. et al., "BGA vs. QFP: A Summary of Tradeoffs for Selection of High I/O Components", Surface Mount International Conference Proceedings, Surface Mount International, August 28-September1, 1994, San Jose, California, pp. 181-185.
	AQ	2	Burgos, J. et al., "Achieving Accurate Thermal Characterization Using a CFD Code-- A Case Study of Plastic Packages", IEEE Transactions on Components, Packaging, and Manufacturing Technology Part A, IEEE, December 1995, Vol. 18, No. 4, pp. 732-738.
	AR	2	Chadima, M., "Interconnecting Structure Manufacturing Technology," Ball Grid Array National Symposium, Dallas, Texas, March 29-30, 1995.

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	APPLICANT Khan *et al.*	
	FILING DATE December 18, 2001	GROUP 2811

U.S. PATENT DOCUMENTS

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	AA3						
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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ3						Yes No
	AK3						Yes No
	AL3						Yes No
	AM3						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	3	Chanchani, R. et al., "Mini BGA: Pad and Pitch Ease Die Test and Handling", Advanced Packaging, IHS Publishing Group, May/June 1995, pp.34, 36-37.
	AO	3	Chung, T.C. et al., "Rework of Plastic, Ceramic, and Tape Ball Grid Array Assemblies", Ball Grid Array National Symposium Proceedings, Dallas, Texas, March 29-30, 1995, pp. 1-15.
	AP	3	Cole, M.S. and Caulfield, T. "A Review of Available Ball Grid Array (BGA) Packages", Journal of Surface Mount Technology, Surface Mount Technology Association, January 1996, Vol. 9, pp. 4-11.
	AQ	3	Cole, M.S. and Caulfield, T., "Ball Grid Array Packaging", Surface Mount International Conference Proceedings, Surface Mount International, August 28-September1, 1994, San Jose, California, pp. 147-153.
	AR	3	Dobers, M. and Seyffert, M., "Low Cost MCMs: BGAs Provide a Fine-Pitch Alternative", Advanced Packaging, IHS Publishing Group, September/October 1994, Vol. 3, No. 5, pp. 28, 30 and 32.

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	APPLICANT Khan *et al.*	
	FILING DATE December 18, 2001	GROUP 2811

U.S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ4						Yes No
	AK4						Yes No
	AL4						Yes No
	AM4						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	4	Dody, G. and Burnette, T., "BGA Assembly Process and Rework", Journal of Surface Mount Technology, Surface Mount Technology Association, January 1996, Vol. 9, pp. 39-45.
	AO	4	Edwards, D. et al., "The Effect of Internal Package Delaminations on the Thermal Performance of PQFP, Thermally Enhanced PQFP, LOC and BGA Packages", 45th Electronic Components & Technology Conference, IEEE, May 21-24, 1995, Las Vegas, NV, pp. 285-292.
	AP	4	Ejim, T.L. et al., "Designed Experiment to Determine Attachment Reliability Drivers for PBGA Packages", Journal of Surface Mount Technology, Surface Mount Technology Association, January 1996, Vol. 9, pp. 30-38.
	AQ	4	Ewanich, J. et al., "Development of a Tab (TCP) Ball Grid Array Package", Proceedings of the 1995 International Electronics Packaging Conference, San Diego, CA, September 24-27, 1995, pp. 588-594.
	AR	4	Fauser, S. et al, "High Pin-Count PBGA Assembly", Circuits Assembly, February 1995, Vol 6, No. 2, pp. 36-38 and 40.

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1875.1640000	APPLICATION NO. 10/020,207
	APPLICANT Khan et al.	
	FILING DATE December 18, 2001	GROUP 2811

U.S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ5						Yes No
	AK5						Yes No
	AL5						Yes No
	AM5						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	5	Fauser, Suzanne et al., "High Pin Count PBGA Assembly: Solder Defect Failure Modes and Root Cause Analysis", Surface Mount International, Proceedings of The Technical Program, Surface Mount International, August 28-September1, 1994, San Jose, California, pp. 169-174.
	AO	5	Ferguson, M. "Ensuring High-Yield BGA Assembly", Circuits Assembly, February 1995, Vol. 6, No. 2, pp. 54, 56 and 58.
	AP	5	Freda, M., "Laminate Technology for IC Packaging", Electronic Packaging & Production, Cahners Publishing Company, October 1995, Vol. 35, No. 11, pp. S4-S5.
	AQ	5	Freedman, M., "Package Size and Pin-Out Standardization", Ball Grid Array National Symposium, March 29-30, 1995, 7 pages.
	AR	5	Freyman, B. and Pennisi, R., "Over-molded Plastic Pad Arrary Carriers (OMPAC): A Low Cost, High Interconnect Density IC Packaging Solution for Consumer and Industrial Electronics", 41st Electronic Components & Technology Conference, IEEE, May 11-16, 1991, pp. 176-82.

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1875.1640000	APPLICATION NO. 10/020,207
	APPLICANT Khan et al.	
	FILING DATE December 18, 2001	GROUP 2811

U.S. PATENT DOCUMENTS

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	AA6						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ6						No
	AK6						Yes No
	AL6						Yes No
	AM6						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	6	Freyman, B. et al., "Surface Mount Process Technology for Ball Grid Array Packaging", Surface Mount International Conference Proceedings, Surface Mount International, August 29-September 2, 1993, San Jose, California, pp. 81-85.
	AO	6	Freyman, B. et al., "The Move to Perimeter Plastic BGAs", Surface Mount International Conference Proceedings, San Jose, CA, August 29-31, 1995, pp. 373-382.
	AP	6	Freyman, B., "Trends in Plastic BGA Packaging," Ball Grid Array National Symposium, Dallas, Texas, March 29-30, 1995, 45 pages.
	AQ	6	Gilleo, K., "Electronic Polymers: Die Attach and Oriented Z-Axis Films", Advanced Packaging, IHS Publishing Group, September/October 1994, Vol. 3, No. 5, pp. 37-38, 40 and 42.
	AR	6	Guenin, B. et al., "Analysis of a Thermally Enhanced Ball Grid Array Package", IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part A, IEEE Components, Packaging, and Manufacturing Technology Society, December 1995, Vol. 18, No. 4, pp. 749-757.

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FORM PTO-1449 ~~INFORMATION DISCLOSURE STATEMENT~~	ATTY. DOCKET NO. 1875.1640000	APPLICATION NO. 10/020,207
	APPLICANT Khan *et al.*	
	FILING DATE December 18, 2001	GROUP 2811

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA7						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ7						Yes No
	AK7						Yes No
	AL7						Yes No
	AM7						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	7	Hart, C., "Vias in Pads for Coarse and Fine Pitch Ball Grid Arrays", Surface Mount International Conference Proceedings, Surface Mount International, August 28-September1, 1994, San Jose, California, pp. 203-207.
	AO	7	Hart, C. "Vias in Pads", Circuits Assembly, February 1995, Vol. 6, No. 2, pp. 42, 44-46 and 50.
	AP	7	Hattas, D., "BGAs Face Production Testing: New Package Offers Promise but Must Clear Technology Hurdles.", Advanced Packaging, IHS Publishing Group, Summer 1993, Vol. 2, No. 3, pp. 44-46.
	AQ	7	Heitmann, R., "A Direct Attach Evolution: TAB, COB and Flip Chip Assembly Challenges", Advanced Packaging, IHS Publishing Group, July/August 1994, Vol. 3, No. 4, pp. 95-99 and 103.
	AR	7	Hodson, T., "Study Examines BGA Use", Electronic Packaging & Production, March 1993, page unknown.

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	APPLICANT Khan *et al.*	
	FILING DATE December 18, 2001	GROUP 2811

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA8						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ8						Yes No
	AK8						Yes No
	AL8						Yes No
	AM8						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	8	Holden, H., "The Many Techniques of Small Via Formation for Thin Boards", The Institute for Interconnecting and Packaging Electronic Circuits Ball Grid Array National Symposium, San Diego, CA, January 18-19, 1996, pp. 1-7.
	AO	8	Houghten, J., "New Package Takes On QFPs", Advanced Packaging, IHS Publishing Group, Winter 1993, Vol. 2, No. 1, pp. 38-39.
	AP	8	"How To Give Your BGAs A Better Bottom Line.", Advanced Packaging, IHS Publishing Group, January/February 1995, page unknown.
	AQ	8	Huang, W. and Ricks, J.,"Electrical Characterization of PBGA for Communication Applications by Simulation and Measurement", National Electronic Packaging and Production Conference West '95, February 26-March 2, 1995, Anaheim, California, pp. 300-307.
	AR	8	Hundt, M. et al., "Thermal Enhancements of Ball Grid Arrays", National Electronic Packaging and Production Conference West '95, Reed Exhibition Companies, Anaheim, CA, February 25-29, 1996, pp. 702-711.

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	APPLICANT Khan *et al.*	
	FILING DATE December 18, 2001	GROUP 2811

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA9						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ9						Yes No
	AK9						Yes No
	AL9						Yes No
	AM9						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	9	Hutchins, C.L., "Understanding Grid Array Packages", Surface Mount Technology Magazine, IHS Publishing Group, November 1994, Vol. 8, No. 11, pp. 12-13.
	AO	9	Hwang, J.S., "Reliability of BGA Solder Interconnections", Surface Mount Technology Magazine, IHS Publishing Group, September 1994, Vol. 8, No. 9, pp. 14-15.
	AP	9	Hwang, J.S., "A Hybrid of QFP and BGA Architectures", Surface Mount Technology Magazine, IHS Publishing Group, February 1995, Vol. 9, No. 2, p. 18.
	AQ	9	Johnson, R. et al., "A Feasibility Study of of Ball Grid Array Packaging", National Electronic Packaging and Production Conference East '93, Boston, Massachusetts, June 14-17, 1993, pp. 413-422.
	AR	9	Johnson, R. et al., "Thermal Characterization of 140 and 225 Pin Ball Grid Array Packages", National Electronic Packaging & Production Conference East '93, Boston, Massachusetts, June 14-17, 1993, pp. 423-430.

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	APPLICANT Khan *et al.*	
	FILING DATE December 18, 2001	GROUP 2811

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA10						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ10						Yes No
	AK10						Yes No
	AL10						Yes No
	AM10						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	10	Johnston, P., "Land Pattern Interconnectivity Schemes", Ball Grid Array National Symposium, Dallas, Texas, March 29-30, 1995, pages 2-21.
	AO	10	Johnston, P. "Printed Circuit Board Design Guidelines for Ball Grid Array Packages", Journal of Surface Mount Technology, Surface Mount Technology Association, January 1996, Vol. 9, pp. 12-18.
	AP	10	Kawahara, T. et al., "Ball Grid Array Type Package By Using of New Encapsulation Method", Proceedings of the 1995 International Electronics Packaging Conference, San Diego, CA, September 24-27, 1995, pp. 577-587.
	AQ	10	Knickerbocker, J.U. and Cole, M.S., "Ceramic BGA: A Packaging Alternative", Advanced Packaging, IHS Publishing Group, January/February 1995, Vol. 4, No. 1, pp. 20, 22 and 25.
	AR	10	Kromann, G., et al., "A Hi-Density C4/CBGA Interconnect Technology for a CMOS Microprocessor", National Electronic Packaging and Production Conference West '95, IEEE, February 26-March 2, 1995, Anaheim, California, pp. 1523-1529.

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	APPLICANT Khan *et al.*	
	FILING DATE December 18, 2001	GROUP 2811

U.S. PATENT DOCUMENTS

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	AA11						
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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ11						Yes No
	AK11						Yes No
	AL11						Yes No
	AM11						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	11	Kunkle, R., "Discrete Wiring for Array Packages", Ball Grid Array National Symposium, Dallas, Texas, March 29-30, 1995, 9 pages.
	AO	11	Lall, B. et al, "Methodology for Thermal Evaluation of Multichip Modules", IEEE Transactions on Components, Packaging, and Manufacturing Technology Part A, IEEE, December 1995, Vol. 18, No. 4, pp. 758-764.
	AP	11	Lasance, C. et al., "Thermal Characterization of Electronic Devices with Boundary Condition Independent Compact Models", IEEE Transactions on Components, Packaging, and Manufacturing Technology Part A, IEEE Components, Packaging, and Manufacturing Technology Society, December 1995, Vol. 18, No. 4, pp. 723-731.
	AQ	11	Lau, J., "Ball Grid Array Technology", McGraw-Hill Inc., 1995, entire book submitted.
	AR	11	Lau, J. et al., "No Clean Mass Reflow of Large Plastic Ball Grid Array Packages", Circuit World, Wela Publications Ltd., Vol. 20, No. 3, March 1994, pp.15-22.

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	APPLICANT Khan *et al.*	
	FILING DATE December 18, 2001	GROUP 2811

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA12						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ12						Yes No
	AK12						Yes No
	AL12						Yes No
	AM12						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	12	"Literature Review", Special Supplement to Electronic Packaging & Production, February 1995, Cahners Publication, 10 pages.
	AO	12	LSI LOGIC Package Selector Guide, Second Edition, LSI Logic Corporation, 1994-1995, entire document submitted.
	AP	12	"LTCC MCMs Lead to Ceramic BGAs," Advanced Packaging, IHS Publishing Group, September/October 1994, Vol. 3, No. 5, pp. 14-15.
	AQ	12	Mak, Dr. W.C. et al., "Increased SOIC Power Dissipation Capability Through Board Design and Finite Element Modeling", Journal of Surface Mount Technology, Surface Mount International, October 1994, pp. 33-41.
	AR	12	Marrs, R.C. and Olachea, G., "BGAs For MCMs: Changing Markets and Product Functionality", Advanced Packaging, IHS Publishing Group, September/October 1994, Vol. 3, No. 5, pp. 48, 50, and 52.

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	APPLICANT Khan *et al.*	
	FILING DATE December 18, 2001	GROUP 2811

U.S. PATENT DOCUMENTS

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	AA13						
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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ13						Yes No
	AK13						Yes No
	AL13						Yes No
	AM13						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	13	Matthew, L.C. et al., "Area Array Packaging: KGD in a Chip-Sized Package", Advanced Packaging, IHS Publishing Group, July/August 1994, pp. 91-94.
	AO	13	Mawer, A. et al., "Plastic BGA Solder Joint Reliability Considerations", Surface Mount International Conference Proceedings, Surface Mount International, August 28-September1, 1994, San Jose, California, pp. 239-251.
	AP	13	Mazzullo, T. and Schaertl, L., "How IC Packages Affect PCB Design", Surface Mount Technology Magazine, February 1995, Vol. 9, No. 2, pp. 114-116.
	AQ	13	Mearig, J., "An Overview of Manufacturing BGA Technology", National Electronic Packaging and Production Conference West '95, February 26-March 2, 1995, Anaheim, California, pp. 295-299.
	AR	13	Mertol, A., "Application of the Taguchi Method on the Robust Design of Molded 225 Plastic Ball Grid Array Packages", IEEE Transactions on Components, Packaging, and Manufacturing Technology Part B: Advanced Packaging, IEEE, November 1995, Vol. 18, No. 4, pp. 734-743.

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	APPLICANT Khan et al.	
	FILING DATE December 18, 2001	GROUP 2811

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
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	AJ14						Yes No
	AK14						Yes No
	AL14						Yes No
	AM14						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	14	Mescher, P. and Phelan, G., "A Practical Comparison of Surface Mount Assembly for Ball Grid Array Components", Surface Mount International Conference Proceedings, Surface Mount International, August 28-September1, 1994, San Jose, California, pp. 164-168.
	AO	14	Mulgaonker, S. et al., "An Assessment of the Thermal Performance of the PBGA Family", Eleventh Annual IEEE Semiconductor Thermal Measurement and Management Symposium, IEEE, San Jose, CA, February 7-9, 1995,pp. 17-27.
	AP	14	"New PBGA Pushes Technology to Outer Limits", Advanced Packaging, IHS Publishing Group, January/February 1995, page 11.
	AQ	14	Olachea, G., "Managing Heat: A Focus on Power IC Packaging", Electronic Packaging & Production (Special Supplement), Cahners Publishing Company, November 1994, pp. 26-28.
	AR	14	"Pad Array Improves Density", Electronic Packaging & Production, Cahners Publishing Company, May 1992, pp. 25-26.

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1875.1640000	APPLICATION NO. 10/020,207
	APPLICANT Khan *et al.*	
	FILING DATE December 18, 2001	GROUP 2811

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA15						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ15						Yes No
	AK15						Yes No
	AL15						Yes No
	AM15						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	15	Partridge, J. and Viswanadham, P., "Organic Carrier Requirements for Flip Chip Assemblies", Journal of Surface Mount Technology, Surface Mount Technology Association, July 1994, pp. 15-20.
	AO	15	Ramirez, C. and Fauser, S., "Fatigue Life Comparison of The Perimeter and Full Plastic Ball Grid Array", Surface Mount International Conference Proceedings, Surface Mount International, August 28-September1, 1994, San Jose, California, pp. 258-266.
	AP	15	Rogren, P., "MCM-L Built on Ball Grid Array Formats", National Electronic Packaging and Production Conference West '94, Anaheim, California, pp. 1277-1282.
	AQ	15	Rooks, S., "X-Ray Inspection of Flip Chip Attach Using Digital Tomosynthesis", Surface Mount International, Proceedings of The Technical Program, August 28-September1, 1994, San Jose, California, pp. 195-202.
	AR	15	Rukavina, J., "Attachment Methodologies: Ball Grid Array Technology", Ball Grid Array National Symposium, Dallas, Texas, March 29-30, 1995, 37 pages.

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	AA16						
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	AJ16						Yes No
	AK16						Yes No
	AL16						Yes No
	AM16						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	16	Sack, T., "Inspection Technology", Ball Grid Array National Symposium, Dallas, Texas, March 29-30, 1995, pages 1-41.
	AO	16	Sakaguchi, H., "BGA MountingTechnology," pgs. 1-4, date and source unknown.
	AP	16	Schmolze, C. and Fraser, A., "SPICE Modeling Helps Enhance BGA Performance", Electronic Packaging & Production, January 1995, pp. 50-52.
	AQ	16	Semiconductor Group Package Outlines Reference Guide, Texas Instruments, 1995, entire document submitted.
	AR	16	Shimizu, J., "Plastic Ball Grid Array Coplanrity", Surface Mount International Conference, San Jose, California, August 31-September 2, 1993, pp. 86-91.

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U.S. PATENT DOCUMENTS

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	AA17						
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	AJ17						Yes No
	AK17						Yes No
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	AM17						Yes No

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	AN	17	Sigliano, R., "Using BGA Packages: An Appealing Technology in a QFP and Fine-Pitch Market", Advanced Packaging, IHS Publishing Group, March/April 1994, pp. 36-39.
	AO	17	Sirois, L., "Dispensing for BGA: Automated Liquid Dispensing in a High-Density Environment", Advanced Packaging, IHS Publishing Group, May/June 1995, pp. 38 and 41.
	AP	17	Solberg, V., "Interconnection Structure Preparation: Impact of Material Handling and PCB Surface Finish on SMT Assembly Process Yield", Ball Grid Array National Symposium, Dallas Texas, March 29-30, 1995, 10 pages.
	AQ	17	"Survival of the Fittest", Advanced Packaging, IHS Publishing Group, March/April 1995, page unknown.
	AR	17	Tuck, J., "BGA Technology Branches Out", Circuits Assembly, February 1995, Vol. 6, No. 2, pp. 24, 26, and 28.

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U.S. PATENT DOCUMENTS

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	AJ18						Yes No
	AK18						Yes No
	AL18						Yes No
	AM18						Yes No

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	AN	18	"Tutorial and Short Courses", 45th Electronic Components & Technology Conference, May 21-24, 1995, Las Vegas, Nevada, IEEE, 6 pages.
	AO	18	Vardaman, E. J. and Crowley, R.T., "Worldwide Trends In Ball Grid Array Developments", National Electronic Packaging and Production Conference West '96, Reed Exhibition Companies, Anaheim, CA, February 25-29, 1996, pp. 699-701.
	AP	18	Walshak, D. and Hashemi, H., "Thermal Modeling of a Multichip BGA Package", National Electronic Packaging and Production Conference West '94, Reed Exhibition Companies, Anaheim, California, February 27-March 4, 1994, pp. 1266-1276.
	AQ	18	Walshak, D. and Hashemi, H., "BGA Technology: Current and Future Direction for Plastic, Ceramic and Tape BGAs", Surface Mount International Conference Proceedings, Surface Mount International, August 28-September1, 1994, San Jose, California, pp. 157-163.
	AR	18	Xie, H. et al., "Thermal Solutions to Pentium Processors in TCP in Notebooks and Sub-Notebooks", 45th Electronic Components & Technology Conference, IEEE, Las Vegas, NV, May 21-24, 1995, pp. 201-210.

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	AJ19						Yes No
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	AL19						Yes No
	AM19						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	19	Yip, W.Y., "Package Characterization of a 313 Pin BGA", National Electronic Packaging and Production Conference West '95, Reed Exhibition Companies, February 26-March 2, 1995, Anaheim, California, pp. 1530-1541.
	AO	19	Zamborsky, E., "BGAs in the Assembly Process", Circuits Assembly, February 1995, Vol. 6, No. 2, pp. 60, 62-64.
	AP	19	Zimerman, M., "High Performance BGA Molded Packages for MCM Application", Surface Mount International Conference Proceedings, Surface Mount International, August 28-September1, 1994, San Jose, California, pp. 175-180.
	AQ	19	Zweig, G., "BGAs: Inspect the Process, Not the Product", Electronic Packaging & Production (Special Supplement), Cahners Publishing Company, August 1994 (Supplement), p. 41.
	AR	19	Houghten, J.L., "Plastic Ball-Grid Arrays Continue To Evolve", Electronic Design, February 6, 1995, pp. 141-146.

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U.S. PATENT DOCUMENTS

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	AJ20						Yes No
	AK20						Yes No
	AL20						Yes No
	AM20						Yes No

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	AN	20	Marrs, R. et al., "Recent Technology Breakthroughs Achieved with the New *Super*BGA® Package", 1995 International Electronics Packaging Conference, San Diego, California, September 24-27, 1995, pp. 565-576.
	AO	20	Hayden, T.F. et al., "Thermal & Electrical Performance and Reliability Results for Cavity-Up Enhanced BGAs", Electronic Components and Technology Conference, IEEE,1999, pp. 638-644.
	AP	20	Thompson, T., "Reliability Assessment of a Thin (Flex) BGA Using a Polyimide Tape Substrate", International Electronics Manufacturing Technology Symposium, IEEE, 1999, pp. 207-213.
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	AR	20	

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